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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 09/817,473 03/26/01 |

Y. Xu, J.Z. Zheng, Jane C.M. Hui,
C. Lin, Y.S. Lin

GAP FILLING PROCESS IN INTEGRATED
CIRCUITS USING LOW DIELECTRIC
CONSTANT MATERIALS

| Grp. Art Unit: |
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INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

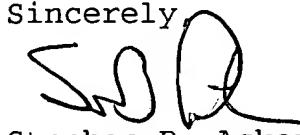
U.S. Patent 5,818,111 to Jeng et al., "Low Capacitance
Interconnect Structures in Integrated Circuits using a Stack of
Low Dielectric Materials", describes a method and structure for
integrating hydrogen silsesqui-oxane (HSQ) and other low
dielectric materials, which have undesirable properties, into
integrated circuit structures and processes.

U.S. Patent 5,759,906 to Lou, "Planarization Method for Intermetal Dielectrics between Multilevel Interconnections on Integrated Circuits", describes a method for making a planar intermetal dielectric layer (IMD) for multilevel electrical interconnections on ULSI circuits.

U.S. Patent 5,385,866 to Bartush, "Polish Planarizing using Oxidized Boron Nitride as a Polish Stop", describes a method of polishing of a non-planar surface layer on a semiconductor substrate using an oxidized boron nitride polishing stop layer.

U.S. Patent 5,821,621 to Jeng, "Low Capacitance Interconnect Structure for Integrated Circuits", describes a method for integrating polymer and other low dielectric constant materials, which may have undesirable physical properties, into integrated circuits structures and processes, especially those requiring multiple levels of interconnect lines.

Sincerely,



Stephen B. Ackerman, Reg. #37761